WHAT IS CLAIMED IS

1. A method for operating a CMOS image sensor including a matrix of pixels arranged in a plurality of lines and columns, each of said pixels including a photosensor element accumulating charge carriers in proportion to the illumination thereof and storage means able to be coupled to said photosensor element at a determined instant in order to generate a sampled signal representative of said charge carriers accumulated by said photosensor, said storage means being intended to assure storage for the purpose of reading said sampled signal,

wherein, when reading said sampled signal, stored on said storage means, said photosensor element is held at a voltage such that any charge carrier generated by said photosensor element is drained and thus does not disturb said sampled signal stored on said storage means.

2. A method according to claim 1, wherein it includes:

- a first phase or initialisation phase, during which said photosensor element and said storage means are initialised at a determined initialisation voltage, said photosensor element and said storage means being uncoupled;

- a second phase or exposure phase during which said photosensor element is released from said initialisation voltage and sores charge carrier in proportion to its illumination;

- a third phase or sampling phase during which said storage means, in a first stage, is released from said initialisation voltage, then, in a second stage, is briefly coupled to said photosensor element, thus allowing said sampled signal to be generated and stored in said storage means, and

- a fourth phase or reading phase, during which said photosensor element, in a first stage, is again initialised at said determined initialisation voltage, then, in a second stage, said sampled signal which is stored on said storage means is read.

3. Method according to claim 2, wherein each pixel includes a reverse polarised photodiode forming said photosensor element and at least a first, a second and a third MOS transistor, said photodiode being connected, on one hand, to a first supply voltage and, on the other hand, to the sources of said first and second transistors, the drains of said first and third transistors being connected to a second supply voltage, the drain of said second transistor and the source of said third transistor being connected to each other and forming a memory node of said storage means,

wherein:

- during said first phase, a first initialisation signal and a second initialisation signal applied respectively to the gate of said first and third transistors of each pixel are brought to levels such that, respectively, said photodiode and said memory node are initialised at a determined initialisation voltage, a control signal applied to the gate of said second transistor of each pixel being brought to a level such that said photodiode and said memory node are uncoupled;

- during said second phase, said first initialisation signal is brought to a level such that said photodiode is released from said initialisation voltage and accumulates charge carriers in proportion to its illumination;

- during said third phase, said second initialisation signal, in a first stage, is brought to a level such that said memory node is released from said initialisation voltage, and said control signal, in a second stage, is briefly brought to a level such that said photodiode and said memory node are coupled, thus allowing the sampled signal to be generated and stored on said memory node, and

- during said fourth phase, said first initialisation signal is first brought to a level such that said photodiode is again initialised at said determined initialisation voltage, and said sampled signal, stored on said memory node, is read.

4. A method according to claim 3, wherein each pixel further includes fourth and fifth MOS transistors, the gate, the drain and the source of said fourth transistor being respectively connected to said memory node, to said second supply voltage, and to the drain of said fifth transistor, the source of said fifth transistor supplying a signal representative of the sampled signal present on said memory node when a line selection signal is applied to the gate of said fifth transistor,

wherein during said fourth phase each line of pixels is addressed in succession so as to allow the sampled signals present on the memory nodes of all the pixels in one line to be read.

5. A method according to claim 4, wherein, following each reading of a line of pixels during said fourth phase, said second initialisation signal applied to each third transistor in said line of pixels is brought to a level such that each memory node in said line of pixels is again initialised at said determined initialisation voltage, the signal then present on each memory node in the line of pixels being used to generate a signal representative of the difference between the signal present on each memory node before and after initialisation.

6. A method according to any of claims 3 to 5, wherein the photodiode is formed in an n type well and in that said transistors are n-MOS transistors.

7. A method according to any of the preceding claims, wherein said storage means is formed of a capacitor protected from the light by a metal layer.